IN THE CLAIMS:

1-10 (Cancelled)

11. (Currently Amended) A parallel-serial conversion circuit comprising:

a self-oscillation circuit which self-oscillates at a specific frequency, wherein said self-oscillation circuit starts self-oscillation when it receives a start signal;

a frequency divider which outputs n (where n is an integer of 2 or above) timing signals of mutually different phases based on an output signal of said self-oscillation circuit, wherein said frequency divider counts the number of ~~oscillation~~ oscillations of said self-oscillation circuit and outputs a stop signal when the count reaches the number n;

a control circuit which outputs a first control signal to said self-oscillation circuit, outputs a second control signal to said frequency divider, and controls the operation of said self-oscillation circuit and said frequency divider based on a starting signal and a timing signal output from said frequency divider using the first and second output signals, wherein said control circuit provides a control to stop the self-oscillation of said self-oscillation circuit when said frequency divider ~~output~~ outputs the stop signal; and

a conversion circuit which ~~convert~~ converts n-bit parallel signals into serial signals based on the n timing signals.

12. (Currently Amended) A serial-parallel conversion circuit comprising:

a self-oscillation circuit which self-oscillates at a specified frequency, wherein said self-oscillation circuit starts self-oscillation when it receives a start signal;

a frequency divider which outputs n (where n is an integer of 2 or above) timing signals of mutually different phases based on an output signal of said self-oscillation circuit, wherein said frequency divider counts the number of ~~oscillation~~ oscillations of said self-oscillation circuit and outputs a stop signal when the count reaches the number n;

a control circuit which outputs a first control signal to said self-oscillation circuit, outputs a second control signal to said frequency divider, and controls the operation of said self-oscillation circuit and said frequency divider based on a starting signal and a timing signal output from said frequency divider using the first and second output signals, wherein said control circuit provides a control to stop the self-oscillation of said self-oscillation circuit when said frequency divider ~~output~~ outputs the stop signal; and

a conversion circuit which ~~convert~~ converts serial signals into n-bit parallel signals based on the n timing signals.

13. (Cancelled)